S/N 10/768,612
Docket: CS03-048
Group art unit : __ 2812

July 1, 2004

To: Commissioner of Patents and Trademarks
P.O. Box 1450 Alexandria, VA 22313-1450

Fr: William J. Stoffel Reg. No. 39,390 CUST NO. 30402
PMB 455
1735 Market St - Suite A
Philadelphia, PA 19103

Subject:

S/N 10/768,612
Docket: CS03-048
Group art unit : __ 2812

File Date: 1/30/2004
Inventor: Li et al.

title: A SEMICONDUCTOR DEVICE LAYOUT AND CHANNELING

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO A820 (also PTO-1449), Information Disclosure Citation and references.

CERTIFICATE OF MAILING OR EXPRESS MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail or Express mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on July 1, 2004.

Signature/Date William J. Stoffel July 1, 2004
William J. Stoffel Reg. No. 39,390
Customer number 30402

S/N 10/768,612
Docket: CS03-048
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The following Patents and/or Publication are submitted to comply with the duty to disclose under CFR 1.97-1.99 and 37 CFR 1.56.

Masahi Shima, "<100> Strained-SiGe- channel p-MOSFET with enhanced hole mobility and lower parasitic Resistance", Fujitsu Sci. Tech. J.,39,1, p. 78-83 (June 2003).

Oldiges, et al., " Molecular Dynamics Simulations of LATID implants into Silicon", found on Website http://beam.helsinki.fi/~knordlun/pub/sispad97.pdf ~ 3-1-2004 see http://www.acclab.helsinki.fi/~knordlun/pub/

Brand et al., *Intel's 0.25 micron, 2.0V logic process technology*, Intel Technology Journal Q3,98, pp. 1-4.

Sincerely,

William J. Stoffel
Reg. No. 39,390
Customer number 30,402

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
CS03-048	
Applicant(s)	
Filing Date	**Group Art Unit**
jan 30,2004	

*EXAMINER INITIAL		OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*
		Masahi Shima, "<100> Strained-SiGe- channel p-MOSFET with enhanced hole mobility and lower parasitic Resistance", Fujitsu Sci. Tech. J.,39,1, p. 78-83 (June 2003).
		Oldiges, et al., " Molecular Dynamics Simulations of LATID implants into Silicon", found on Website http://beam.helsinki.fi/~knordlun/pub/sispad97.pdf ~ 3-1-2004 see http://www.acclab.helsinki.fi/~knordlun/pub/
		Brand et al., Intel's 0.25 micron, 2.0V logic process technology, Intel Technology Journal Q3,98, pp. 1-4.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.